UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/008,497	01/16/1998	HIROYUKI INOUE	0433/00547	6301

30678 7590 06/16/2003

CONNOLLY BOVE LODGE & HUTZ LLP
SUITE 800
1990 M STREET NW
WASHINGTON, DC 20036-3425

EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 06/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/008,497	INOUE, HIROYUKI	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,21-32 and 34-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-9,21-32 and 34-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 114, claiming priority from U.S. Patent No. 09/008497 filed on January 16, 1998 which itself claims priority under 35 U.S.C. 119 A-d from Japanese Patent Publication No. 07-319482 filed on 14 November, 1995 from which papers have been placed of record in the file.

Continued Prosecution Application

The request filed on 04/01/2003 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/008,497 is acceptable and a CPA has been established. An action on the CPA follows.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed 01 /15 / 2003 has been entered on April 09, 2003.

Specification

Drawings

The drawings filed on 1/16/ 1998 have been accepted by the draftsperson as previously indicated.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 9 and 21 to 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu (U.S Patent No. 4,994,402 herein after Chiu) OR Matthews (U.S. Patent No. 5,134, 083 herein after Matthews) both previously applied.

With respect to claim 1 Chiu or Matthews describe a method for manufacturing a semiconductor device having a buried conductive layer which is connected to one of a source and drain of a MOS transistor and which extends over a gate electrode of said MOS transistor, said method comprising: (Chiu col.1 line 32, Matthews Abstract lines 2-3)

forming a first insulating film on a semiconductor substrate; (Chiu fig. 1 # 12, 13, Matthews fig. 5 A # 28)

forming a first conductive film as said gate electrode (Chiu fig. 1 # 16 , Matthews fig. 6 A # 26 and a second insulating film on said first insulating film, (Chiu figure 1 # 20, Matthews figure 7 A # 32) said gate electrode having a width equal to a minimum processing size achievable with a lithographic process technique; (Chiu col. 2 lines 13 to 20 Matthews col. 1 lines 43-46)

forming a third insulating film on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film and said second insulating film formed thereon ; (Chiu figures 5-6 etc. and col. 5 lines 48-55, Matthews fig. 9 A).

selectively etching away said third insulating film so as to form a side wall insulating film including said third insulating film on each of both side faces of said first conductive film and said second insulating film and also to expose said semiconductor substrate in portions which are not covered with said side wall insulating film and not covered with said first conductive film; (Chiu figure 6 and Matthews figure 9 A).

diffusing impurities into said exposed portions of said semiconductor substrate so as to form a source and a drain in said semiconductor substrate; (Chiu figure 6, Matthews 10 A).

forming a second conductive film to be a part of said buried conductive layer on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film, said second insulating film and said side wall insulating film formed thereon; forming (Chiu figure 7 # 65, Matthews figure 11 B # 58) a first mask layer on

said second conductive film; (Chiu figures 9, 10, col. 6 line 6 Matthews fig. 11b and 12 A)

processing said first mask layer to have a pattern which is separated into both side portions as to said first conductive film; (Chiu figure 10, Matthews figure 12 A).

forming a second mask layer on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film, said second insulating film, said side wall. insulating film, said second conductive film and said first mask layer formed thereon; (Chiu col.2 lines 61-64, Matthews figure 13 A).

selectively etching away said second mask laver so as to leave a pattern of said second mask layer on each of both side faces of the pattern of said, first mask (Chiu figures 11,1 2 and Matthews (Chiu figure 10, Matthews figure 14 A)

selectively etching away said second conductive film with the patterns of said first and second mask layers as a mask so as to process said second conductive film into a pattern in which said second conductive film is separated on said second insulating film by an opening (Chiu figure 10, Matthews figure 14 A) , said second conductive film which extends over the gate electrode of the MOS transistor. (Chiu figures 11, 12 etc. Matthews figure 19, # 90).

It is noted that Chiu and Matthews may have additional steps in their process , however the instant claims include the term " comprising " that does not exclude additional steps and further current case law states : As a matter of fact selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results (In re Burhaus, 154 F. 2d 6890, 69 USPQ330 (CCPA 1946).

With respect to claims 2 and 4 Matthews in figure 20 A and Chiu in figure 13 disclose a mask layer on an insulating film and a mask on a conductive film.

With respect to claim 3 the recitation of forming two mask layers (See rejection of claim 1 above) .

With respect to claim 5 Chiu col. 7 lines 20-25 and Matthews figs. 16 to 18 disclose two mask layers formed on a conductive film.

With respect to claim 6, it repeats all the steps of claim 1 and then adds the step of forming a wiring layer which is connected to said second conductive film at the bottom of said contact hole . (Chiu fig 12 , plugs 91, 93 , col. 6 lines 66-68, Matthews fig 22 A).

With respect to claims 7 to 9, it repeats all the steps of claim 1 and then adds the step of coating the third conductive film with a dielectric , forming a fourth conductive film and patterning it into a electrode pattern (Matthews fig. 26 A).

Claim 21 repeats the steps of claim 1 and additionally recites the step of having an opening smaller than the minimum processing size (Chiu col. 2 lines 11-20, Matthews col.1 lines 40-52) and also the rejection under claim 1 is incorporated here by reference.

Claim 22 describes the distance between the two conductive layers as l /3 of the minimum processing size feature, the mere recitation of a range without any showing of unexpected results or criticality does not patentably distinguish it over the prior art.

Claim 23 -27,30 the two conductive layers and the mask layer of insulating film is repeated from claim 1.

Claims 28-29 repeat the steps of claims 1, 21 and additionally recites the step of wherein the opposing faces of the atleast two portions extend over a central portion of the gate structure (Chiu figures 8-12, etc., Matthews figure 19 A etc.) and also the rejection under claim 1 is incorporated here by reference.

Claims 31-33 repeat the steps of 28, 29 and 22.

Claims 34 -37 repeat the steps of claim 23 -26 expect for calling the hole in claims 23-26 contact holes in claim 23-26, and the step of said contact hole extending over at least one of the source and drain regions and extending over only a side portion of the gate electrode . (Chiu figures 11, 12 etc. Matthews figure 19, # 90).

Claim 37 repeats the steps of claim 28.

Claim 38 repeats the steps of claim 21including the step of wherein the sidewall spacers are centrally arranged interior to edges of the structure.

Claim 39 repeats the steps of claim 21.

Response to Arguments

Applicants arguments filed January 15, 2003 have been considered, but are not persuasive for the following reasons :

Applicants' first contention that Chiu reference is not directed to feature sizes or holes having dimensions smaller than that achievable by standard photolithographic techniques is not persuasive because Chiu in col. 2 lines 10 to 20 states :

> Methods such as reflow, salicide and planarization have been tried in a continuing effort to solve these problems. However, as the device dimensions have shrunk into the submicron range, these methods have been inadequate to solve all of the problems simultaneously. Accordingly there remains a need for a way to fabricate low-resistance contacts in semiconductor devices having dimensions in the submicron range without suffering the ill effects of junction spiking, high junction capacitance and contact etch stop problems.

Applicants' second argument that Chiu teaches away from the Applicants' disclosed and recited invention is not persuasive because the claims as presently recited do not recite any alignment of holes, similarly the objective/s of the invention are not presently recited in the claims.

Applicants' third argument that Matthews does not acknowledge sub-photolithographic feature sizes in a semiconductor device is not persuasive because Matthews col. 1 lines 42-47 states :

> repeated. Using state-of-the-art optics, projection printing (also frequently referred to as direct-step-on-wafer or step-and-repeat) systems are capable of producing sub-micron resolutions.

Applicants' next contentions that the applied art does not teach/suggest the presently newly added limitations , " which extends over a gate electrode of said MOS transistor" and " wherein the buried conductive layer extends over the gate electrode of the MOS transistor " ; " wherein said sidewalls are formed so as to be between and Offset from end portions of the semiconductor element" ; " said contact hole extending over at least one of the source and drain regions, and extending over only a side portion of the gate electrode " are s not persuasive for reasons stated in the rejections of the claims above.

Dependent claims 2-9,22-27, 29-30, 32, 35-37 and 39 were alleged to be allowable because they depend upon allegedly allowable independent claims.

However as seen above none of the independent claims are allowable therefore the dependent claims are also not allowable.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

June 11, 2003.

SUP[illegible]
TEC[illegible]